nexperia

Discrete Semiconductor Packages

Package miniaturization trend in conflict with application voltage distance requirements

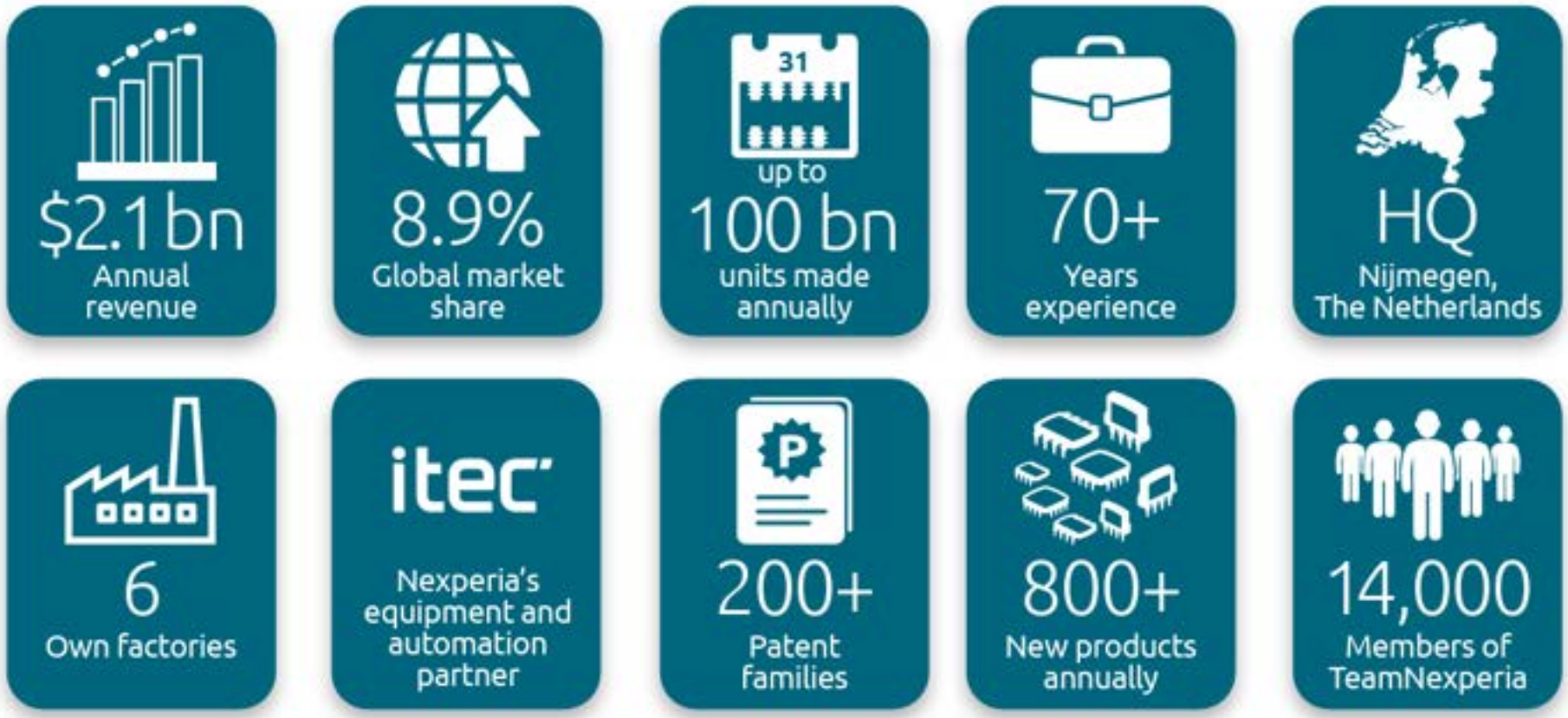
May 2025 • Marc Schikowski

Nexperia

Global semiconductor company

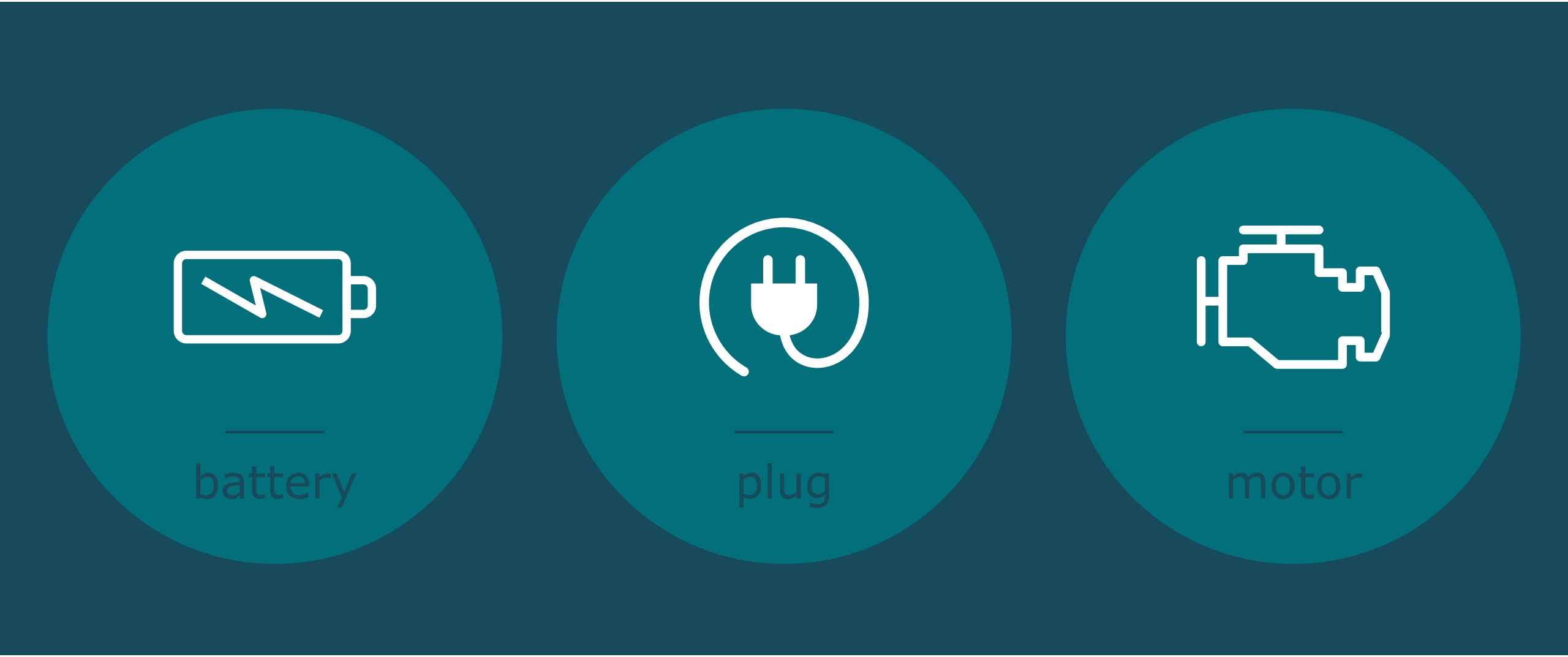
May 2025 • Company Presentation

Key facts



Our essential semiconductors are everywhere

Virtually every electronic design in the world uses Nexperia parts



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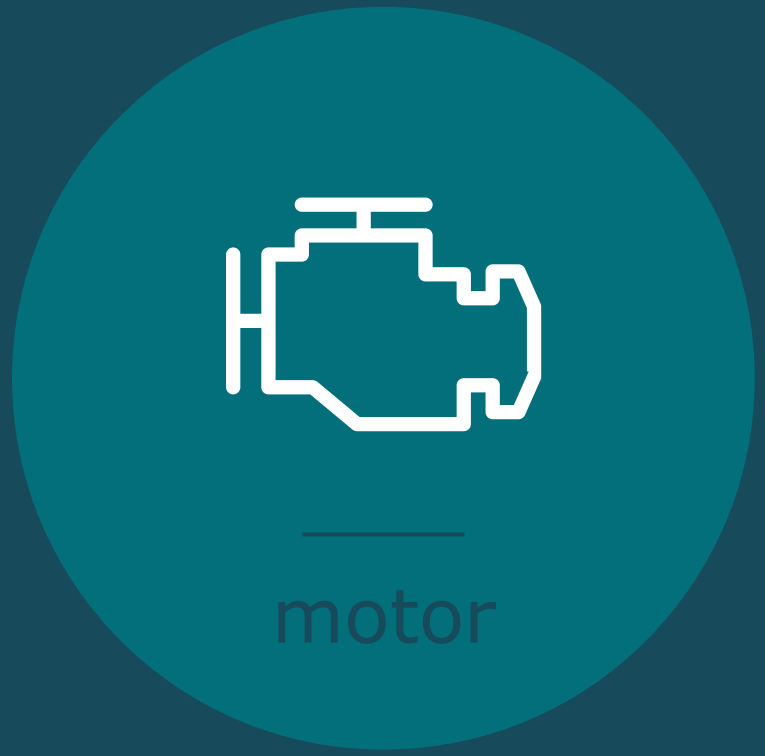

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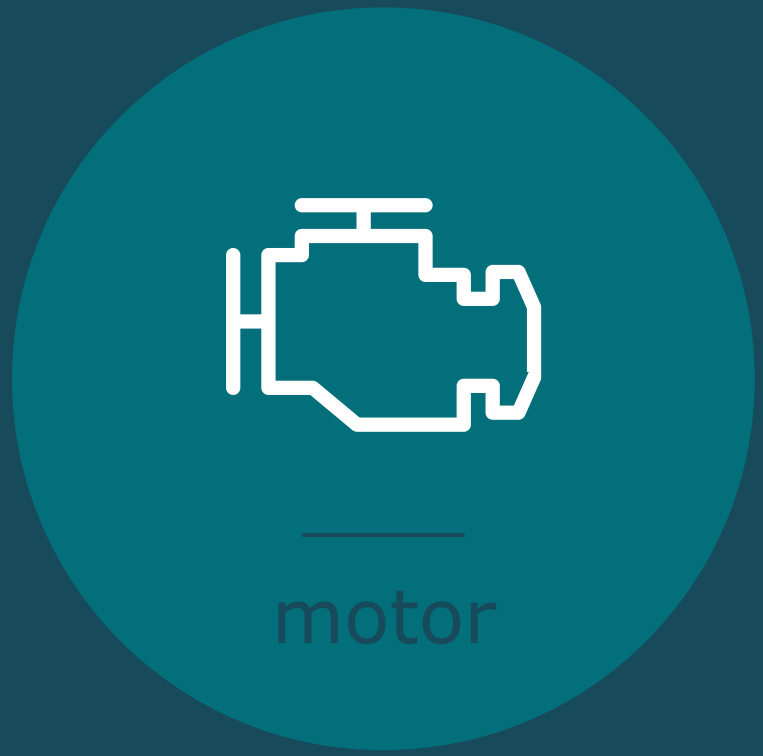

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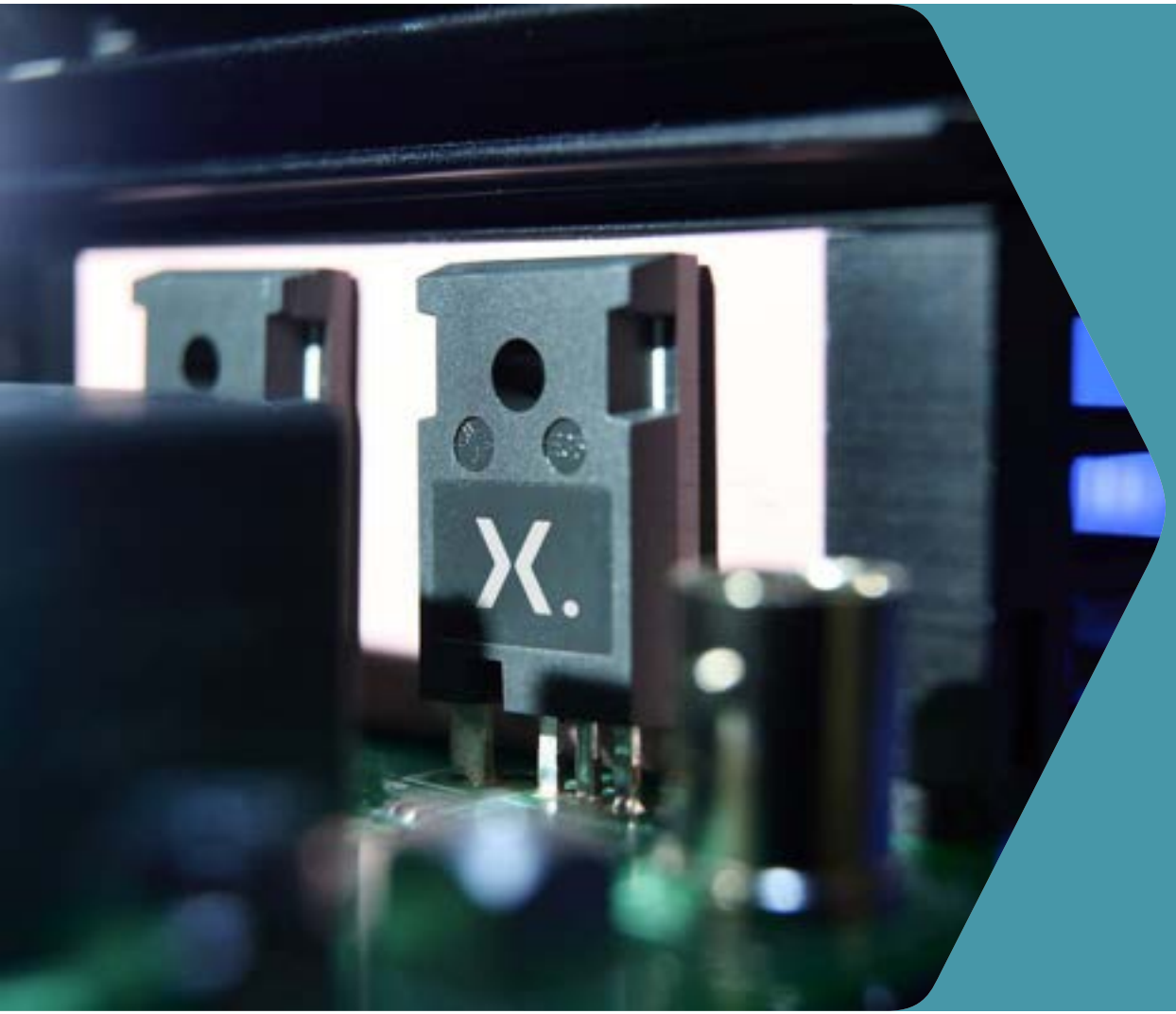
battery

Shaping the future with a diverse and differentiated portfolio



Committed to continued technological innovation and product development

Increased focus and investments in R&D

Accelerate growth and portfolio expansion in Power Discretes, Modules, Analog & Power ICs

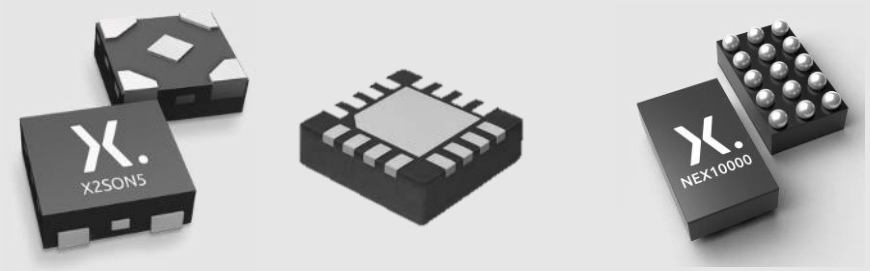
Stronger customer alignment

Building on decades of experience in high volume production and leading market positions

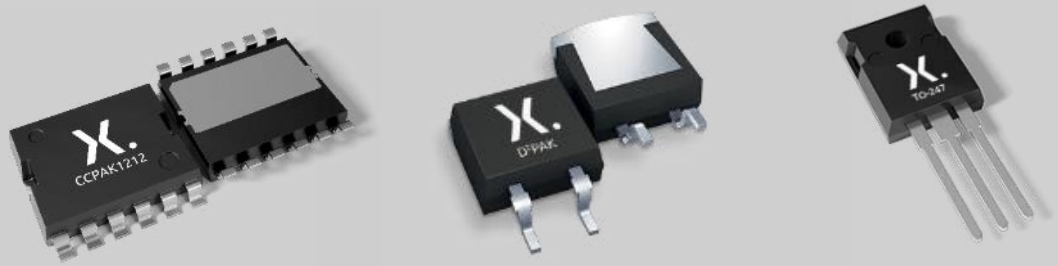
Nexperia Business Groups

Regrouped for increased focus and better alignment to customer needs

IC Solutions

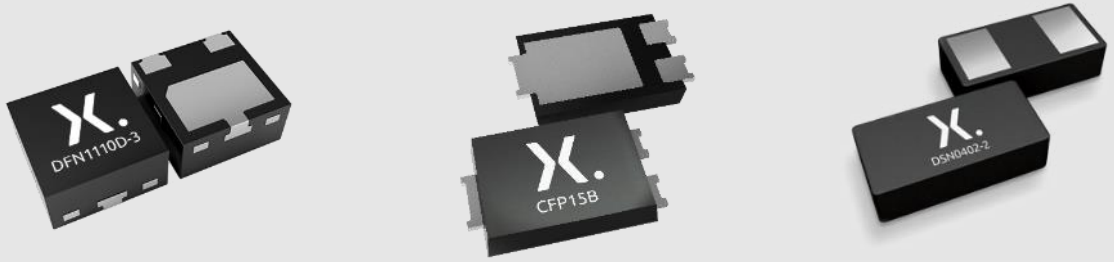


Wide Band Gap, IGBT & Modules

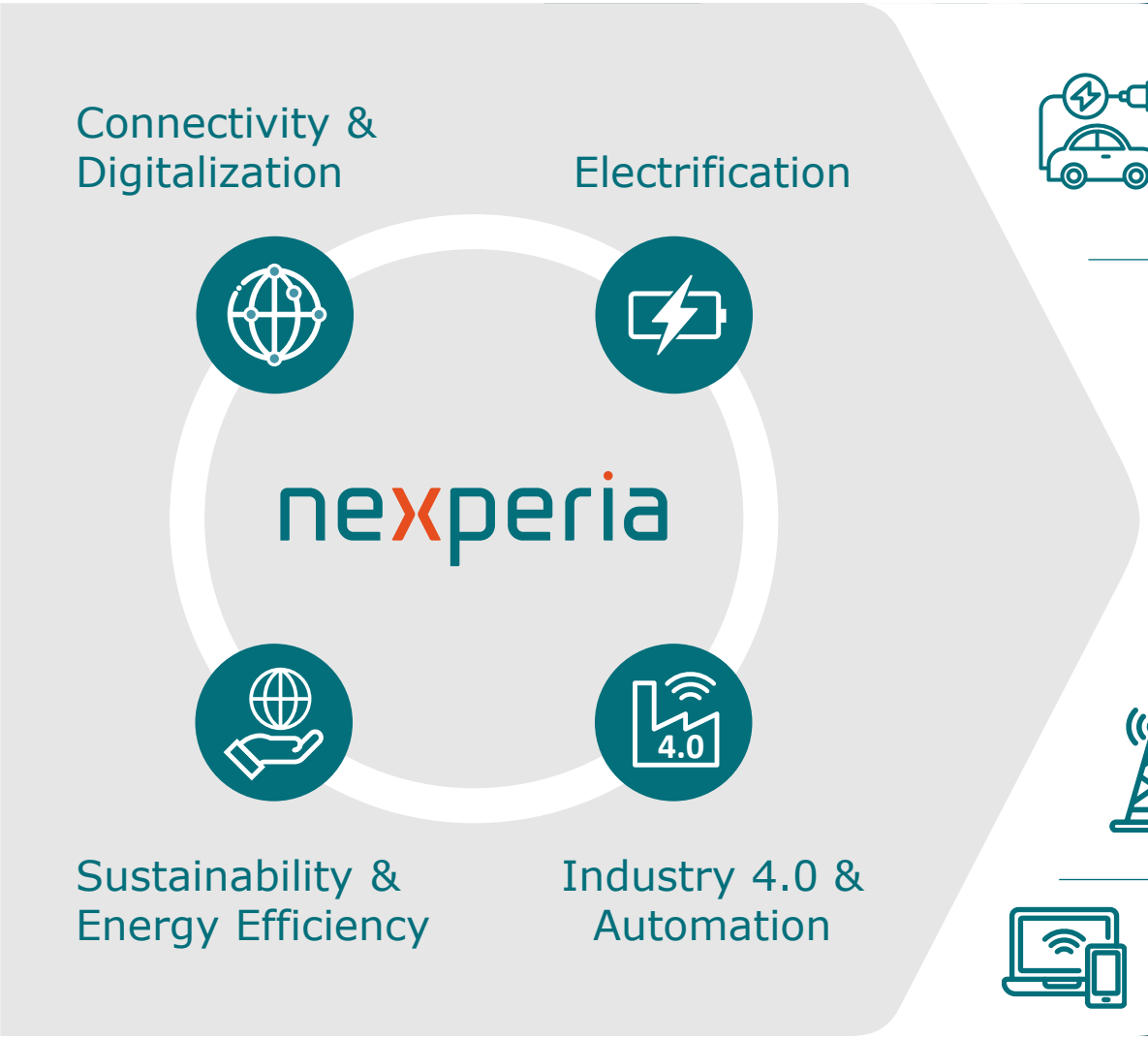


MOS Discretes

Bipolar Discretes



Well positioned to serve the increasing demand from the industry trends



Electrical vehicles require **~3x times** more semiconductors in a power train than in an internal combustion engine car

Urgent need for sustainability and a **successful global energy transition**

Growing need for **power and connectivity**

80% of the global population will have access to **5G and 6G coverage by 2030**

75bn connected devices by 2030

Our best-in-class manufacturing footprint
Vertically integrated - maximum supply chain efficiency & secure capacity

>100 billion products annually

Produced in own wafer fabs and assembly sites supported by long-term foundry and subcon partners

Very high degree of automation in backend factories

Celebrating 100 years in Hamburg in 2024

Exceeding quality standards

A stringent product qualification process aims for Zero Defect performance and AEC-Q101 / 100 for automotive

Quality management system is certified according to ISO 9001, IATF 16949 (automotive)

Product quality is at benchmark level with part per billion (ppb) performance

Preferred supplier status for quality at global players

nexperia

Discrete Semiconductor Packages

Package miniaturization trend in conflict with application voltage distance requirements

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Nexperia Package Platforms

Why package miniaturization?

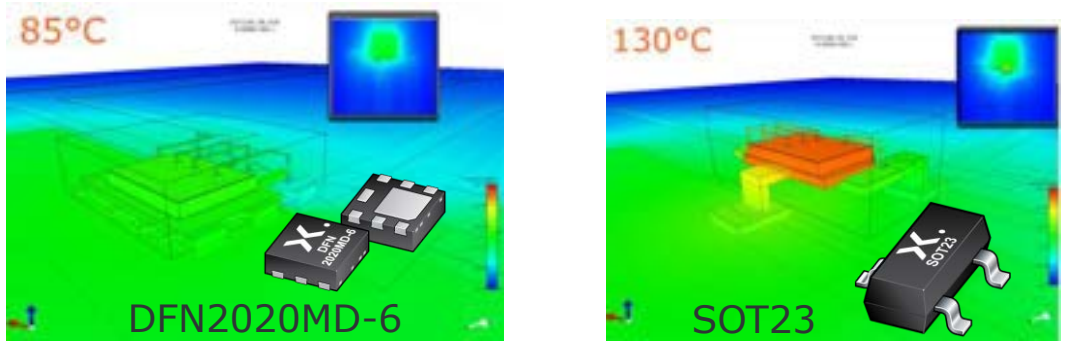
- Better thermals
  - Less mold compound around die
  - Shorter heat dissipation path to PCB substrate
- Better frequency response
  - Less inductance / capacitance
- Less board space
  - More circuitry in same amount of space
  - Lower cost

Why package miniaturization?

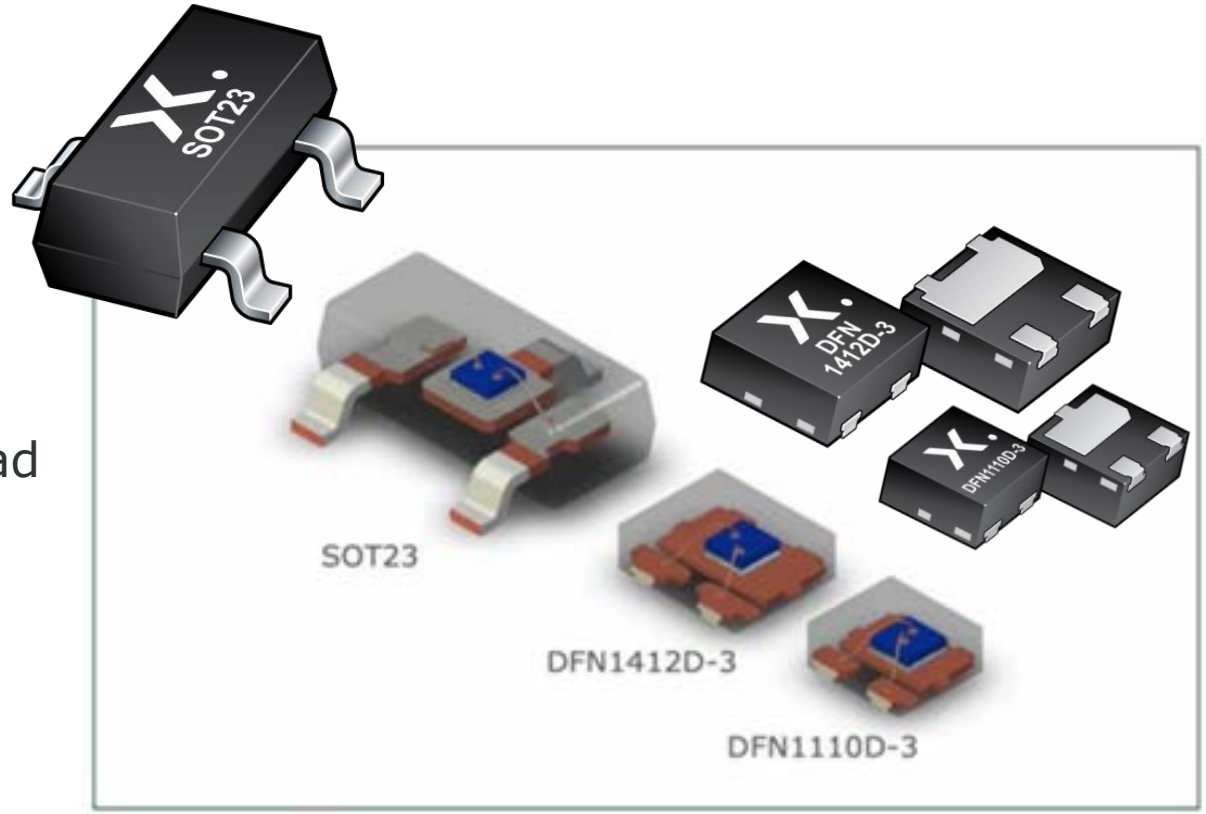
- Better thermals
  - Less mold compound around die
  - Better heat dissipation towards PCB due to
    - Shorter package pads (no gullwing lead)
    - exposed heat sink as dedicated cooling pad

➔ *Same functionality, smaller package, lower $R_{thj\text{-}s}$*

*= **Increased Power Density***



1000 s @ 600 mW: Joule heating of BUK6D22-30E in DFN2020MD-6 vs. PMV15ENEA in SOT23 package



Package	SOT23	DFN1412D-3	DFN1110D-3
Package area	100%	25%	17%
Rthj-s (K/W)	115	53	60

Why package miniaturization?

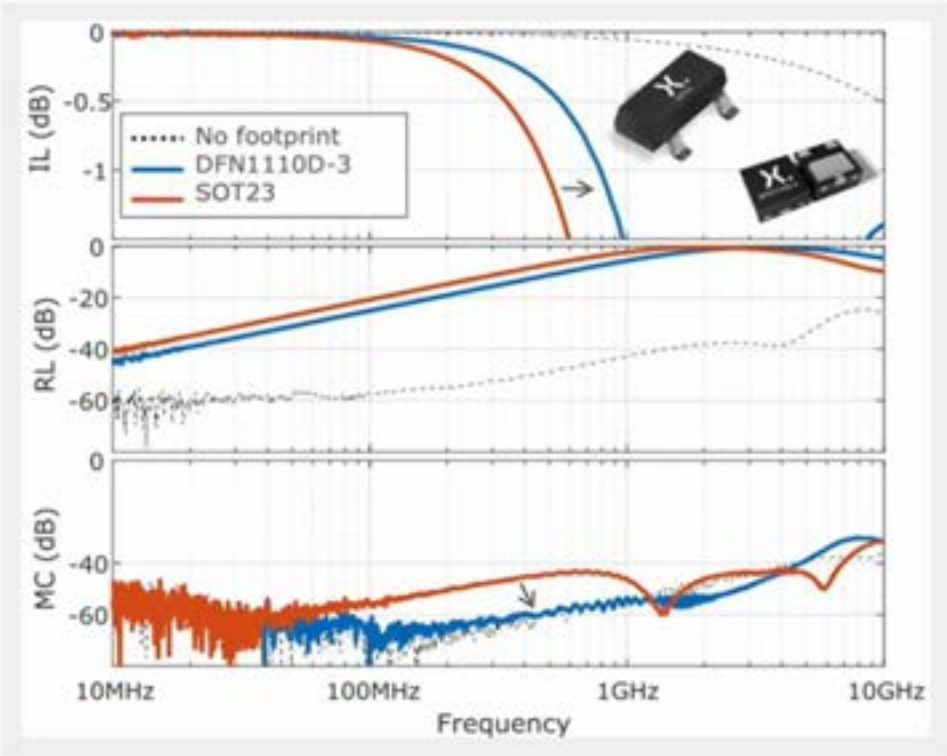
- Better frequency response

High Frequency Performance of smaller packages

Comparison of SOT23 and DFN1110D-3 with PESD2CANFD24V (C_p = 5.2 pF)

Same PCB, dual footprint design

➔ *Same die, smaller package = better performance*

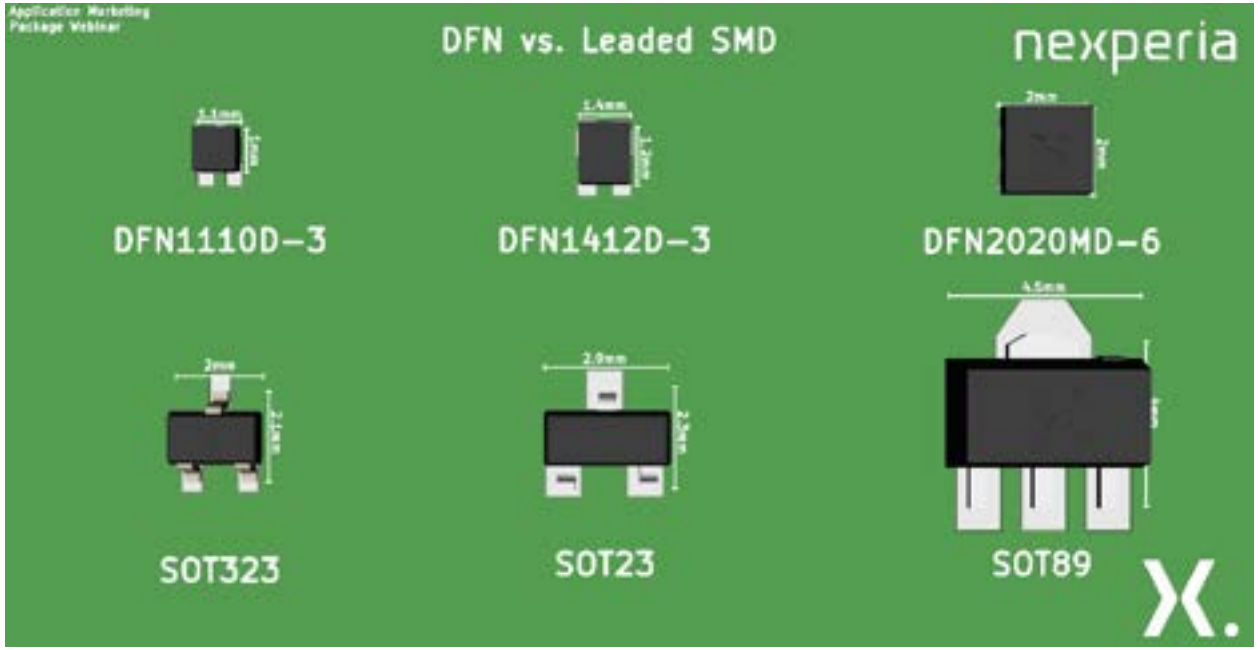


IL = Insertion Loss

RL = Return Loss

Why package miniaturization?

- Less board space
  - More circuitry in same amount of space
  - Enabler for higher power density
  - Lower cost
  - Reduction of product carbon footprint

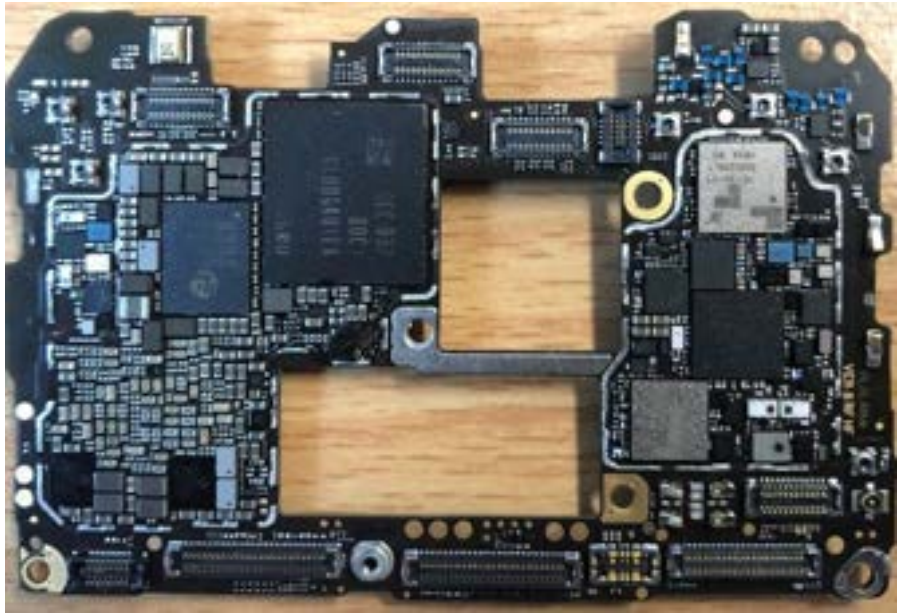


➔ *57-90% of space saving on PCB when selecting DFN counterpart over leaded SMD*

Package miniaturization **vs.** Application voltage distance requirements

More electronics in wide range of applications require higher density in electric circuits

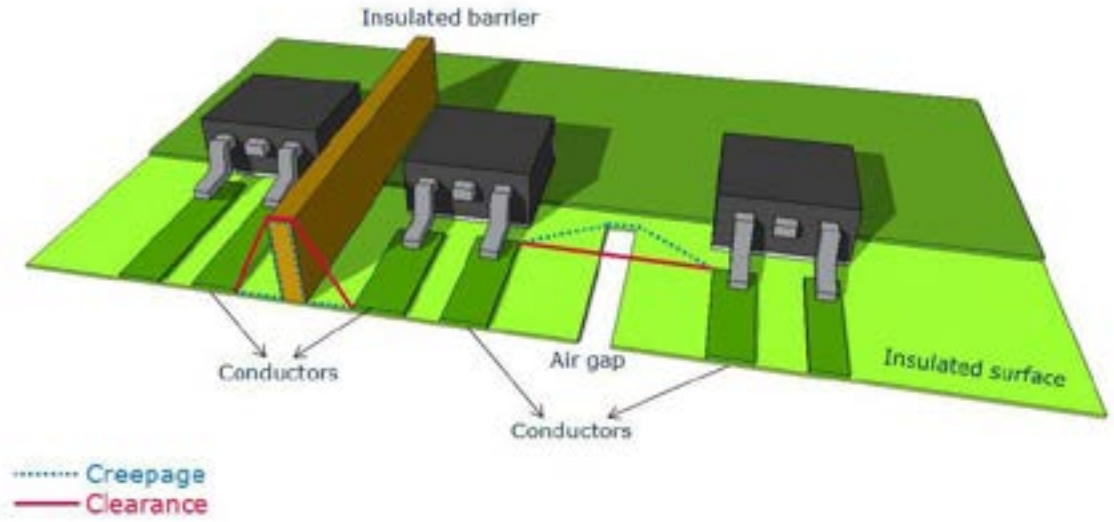
- Smaller packages
- Less distance between metal features



vs.

Clearance/Creepage Distances according to standards (e.g: IEC60664-1 & IPC2221C)

Increasing application voltages,
e.g. in E-mobility: On-board charger (OBC) output to the battery is in the range of 450-850V



IEC60664-1

Insulation coordination for equipment within low-voltage systems

- Table of minimum creepage distances to avoid failure due to tracking
- Typical Automotive application:
- Pollution degree 2
- Material group II

Pollution degrees	Description
Pollution degree 1	No pollution or only dry, non-conductive pollution occurs. The pollution has no influence.
Pollution degree 2	Only non-conductive pollution occurs except that occasionally a temporary conductivity caused by condensation is to be expected.
Pollution degree 3	Conductive pollution occurs or dry non-conductive pollution occurs which becomes conductive due to condensation which is to be expected.
Pollution degree 4	Continuous conductivity occurs due to conductive dust, rain or other wet conditions.

Material groups	Comparative Tracking Index
Material group I	600 ≤ CTI
Material group II	400 ≤ CTI < 600
Material group IIIa	175 ≤ CTI < 400
Material group IIIb	100 ≤ CTI < 175

Table F.4 – Creepage distances to avoid failure due to tracking

Voltage r.m.s. [1]	Minimum creepage distances								
	Printed wiring material		Pollution degree						
	1	2	1	2			3		
	All material groups	All material groups, except IIIb	All material groups	Material group I	Material group II	Material group III	Material group I	Material group II	Material group III [2]
V	mm	mm	mm	mm	mm	mm	mm	mm	mm
10	0,025	0,040	0,080	0,400	0,400	0,400	1,000	1,000	1,000
12,5	0,025	0,040	0,090	0,420	0,420	0,420	1,050	1,050	1,050
16	0,025	0,040	0,100	0,450	0,450	0,450	1,100	1,100	1,100
20	0,025	0,040	0,110	0,480	0,480	0,480	1,200	1,200	1,200
25	0,025	0,040	0,125	0,500	0,500	0,500	1,250	1,250	1,250
32	0,025	0,040	0,14	0,53	0,53	0,53	1,30	1,30	1,30
40	0,025	0,040	0,16	0,56	0,80	1,10	1,40	1,60	1,80
50	0,025	0,040	0,18	0,60	0,85	1,20	1,50	1,70	1,90
63	0,040	0,063	0,20	0,63	0,90	1,25	1,60	1,80	2,00
80	0,063	0,100	0,22	0,67	0,95	1,30	1,70	1,90	2,10
100	0,100	0,160	0,25	0,71	1,00	1,40	1,80	2,00	2,20
125	0,160	0,250	0,28	0,75	1,05	1,50	1,90	2,10	2,40
160	0,250	0,400	0,32	0,80	1,10	1,60	2,00	2,20	2,50
200	0,400	0,630	0,42	1,00	1,40	2,00	2,50	2,80	3,20
250	0,560	1,000	0,56	1,25	1,80	2,50	3,20	3,60	4,00
320	0,75	1,60	0,75	1,60	2,20	3,20	4,00	4,50	5,00
400	1,0	2,0	1,0	2,0	2,8	4,0	5,0	5,6	6,3
500	1,3	2,5	1,3	2,5	3,6	5,0	6,3	7,1	8,0 (7,9) [4]
630	1,8	3,2	1,8	3,2	4,5	6,3	8,0 (7,9) [4]	9,0 (8,4) [4]	10,0 (9,0) [4]
800	2,4	4,0	2,4	4,0	5,6	8,0	10,0 (9,0) [4]	11,0 (9,6) [4]	12,5 (10,2) [4]
1 000	3,2	5,0	3,2	5,0	7,1	10,0	12,5 (10,2) [4]	14,0 (11,2) [4]	16,0 (12,8) [4]

IEC60664-1

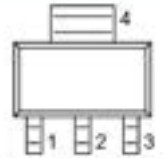
Package distances

IEC60664-1 is not a package standard!

Type	Package	VR, VCE0, VDS in V	smallest external pad to pad distance in mm	smallest feature to feature distance (e.g. Connection bars) in mm	IEC60664 CD in mm
BAS21J	SOD323F	300	1.47	nil	2.2
BAS101	SOT23	300	1.91	nil	2.2
BAW101	SO143B	300	1.87	nil	2.2
BA521	SOD523	300	0.89	nil	2.2
BAW101S	SOT363	300	0.4	nil	2.2
BAS16LD	SOD882D	100	0.4	0.52	1
BAS16	SOT666	100	0.28	nil	1
BAV70M	SOT883	100	0.2	0.205	1
BAS516QA	SOT1215	100	0.175	0.19	1
BAV70SRA	SOT1268	100	0.22	0.3	1
PNS40010ER	SOD123W	400	2.4	nil	2.8
PZTA44	SOT223	400	1.6	nil	2.8
BST39	SOT89	350	1.06	nil	2.6

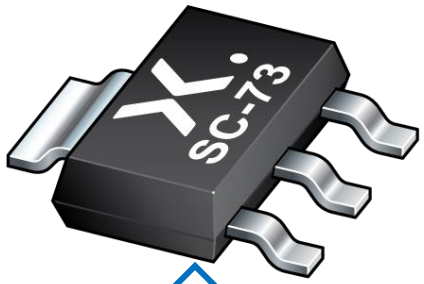
400 V npn high-voltage transistor PZTA44

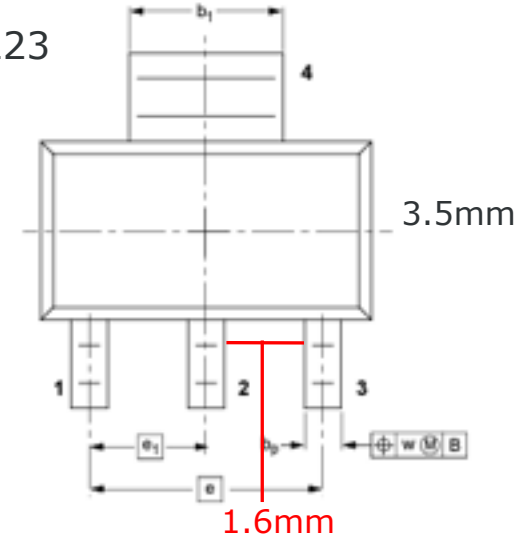
Table 2. Pinning information

Pin	Symbol	Description	Simplified outline
1	B	base	
2	C	collector	
3	E	emitter	
4	C	collector	

SC-73 (SOT223)

Example: SOT223 (SC-73)





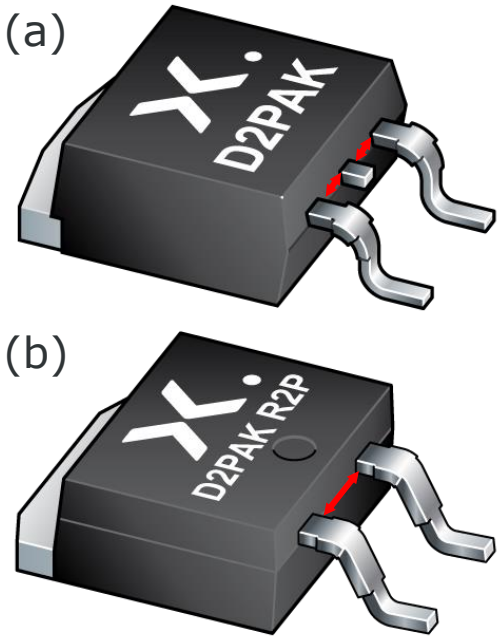
Billions of Products supplied to customers for various applications ➔ **Complaint rate : < 3ppb**

Creepage Distance

Semiconductor SMD packages

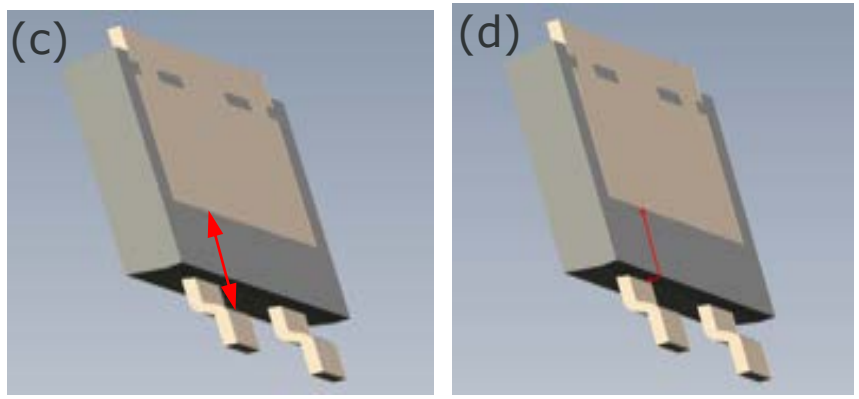
SMD Packages with Real-two-pin (R2P) configuration

- R2P configuration (b) enables larger creepage distance



SMD packages with exposed heat sink:

- Focus is typically distance of heatsink to lead bend area (c)
- This defines distance heatsink solder pad to lead solder pad
- But shortest distance on package needs to be considered (d)
- So package developer needs to consider e.g.
  1. Different lead positioning
  2. Smaller heat sink



Creepage Distance

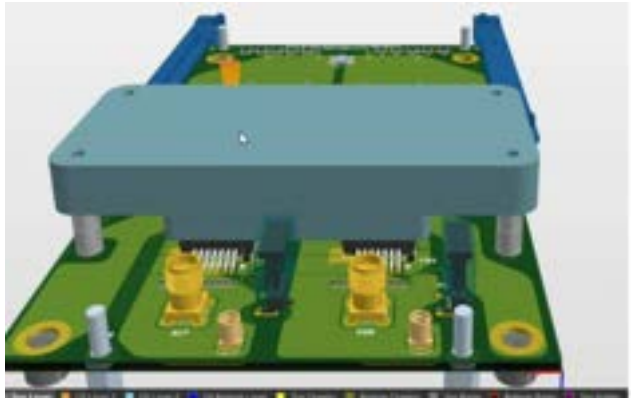
Semiconductor Top side cooled (TSC) packages

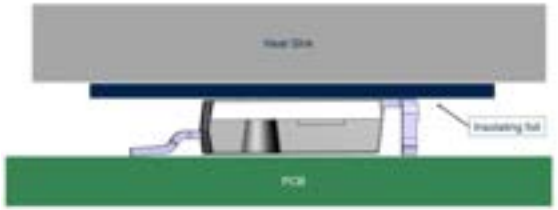
Main motivation for TSC packages

- Separate electrical and thermal path
- Keep advantages of SMT assembly
- Keep PCB temperature low

Product: 1200V SiC MOSFET

- To avoid high voltage on mounted heatsink an insulation foil is used (TIM layer)
- This should as well insulate in respect to creepage distance
- Due to potential imperfect adhesion of TIM layer customers still like to have sufficient creepage distance on package
- So package developer needs to consider e.g.
  1. Use suitable molding compounds (Material Group I)
  2. Increase creepage distance by a groove on plastic body





X.PAK

14 x 19 x 3.5mm^3

CD: 3.7mm

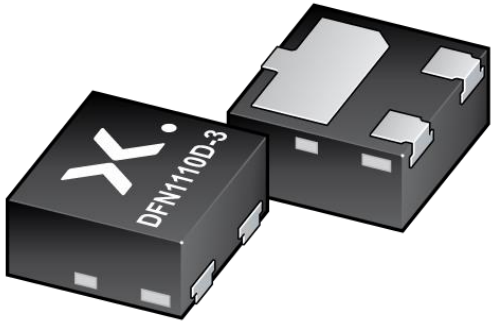
QDPAK

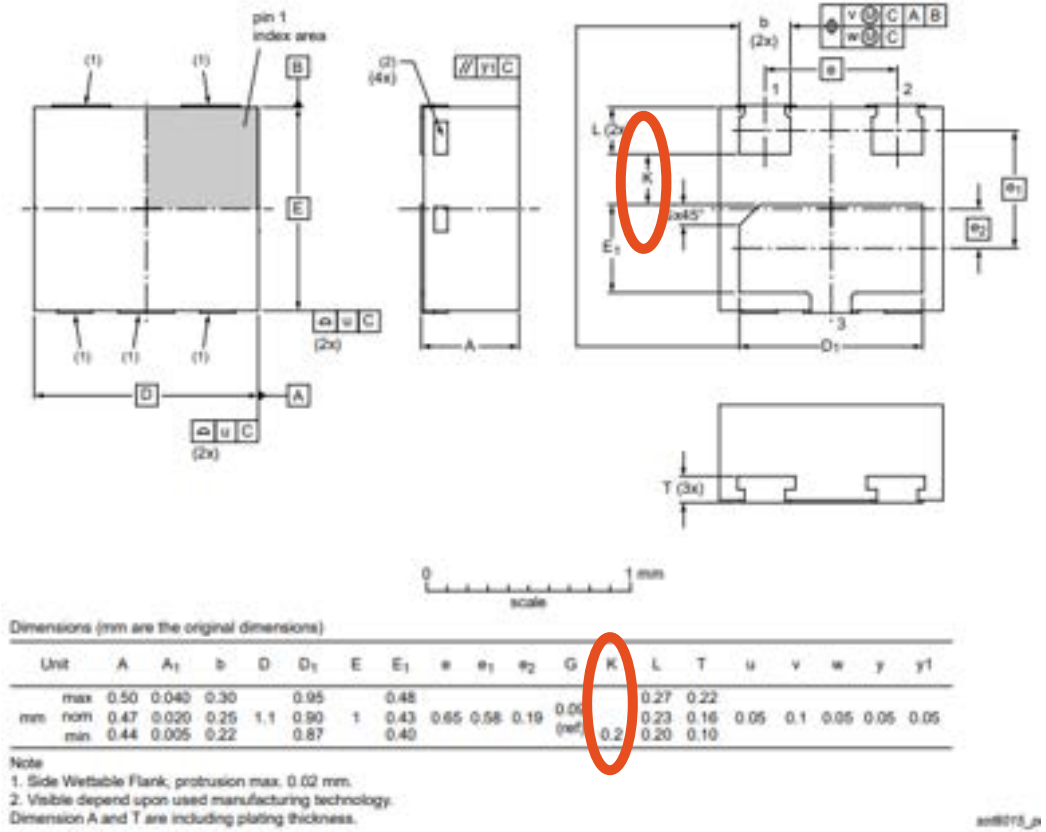
15 x 21 x 2.3mm^3

CD: 4.8mm

The reliability

Example: DFN1110D-3 package with CD of 0.2 mm





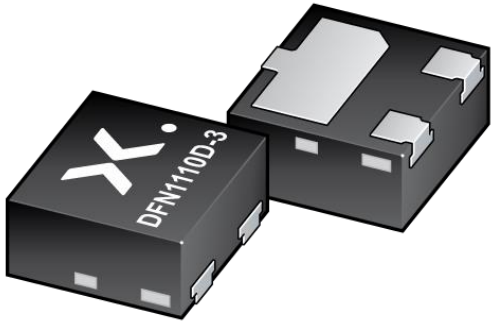
Example of established reliability test:
High **H**umidity **H**igh **T**emperature **R**everse **B**ias (H3TRB): JESD22-A101

- 85°C/85% RH , Reverse Voltage 80% of breakdown voltage
- 1000h / 2000h extended
- Test is done on FR4 PCB

Example Products	Reverse Bias in H3TRB	IEC60664-1 req. creepage distance
BC846AQB-Q, 65V	52V	> 0.9mm
BAV70QB-Q, 100V	80V	>0.95mm

Example of reliability test results

DFN1110D-3 (SOT8015) Qualification Results, Reverse biased Tests



Production Part Approval - Environmental Test Summary

(according to AEC-Q101-Rev-D & AEC-Q006-Rev A)

Supplier	User Part Number (BAV70QB)				
Nexperia	Qualification type: BAV70QB, 3 lots 80V				
Name of Laboratory	**Part Description**				
Quality Hamburg	Dual common cathode high-speed switching diode (SOT8015)				
Test #	**Test Description**	**Test Conditions**	**# Lots**	**# Tested**	**# Failed**
Test Group A - Accelerated Environment Stress Tests					
A1	Preconditioning (PC)	JEDEC/IPC J-STD-020, JESD22-A113, TEST before and after PC, MSL level 1	all[1)]	all[1)]	-
A2	Highly Accelerated Stress Test (HAST)	JEDEC JESD22-A110, T=130°C, 85% RH, t=96 hrs, reverse biased at 80% of rated voltage	_[2)]	-	-
A2 alt	High Humidity High Temperature Reverse Bias (H3TRB)	JEDEC JESD22-A101, Tj=85°C, 85% RH, reverse biased at 80% of rated breakdown voltage (VR=80V), t=2000 hrs	3	77	0
A3	Unbiased Highly Accelerated Stress Test (UHAST)	JEDEC JESD22-A118, Tamb=130°C, 85% RH, t=96 hrs	3	77	0
A3 alt	Autoclave (AC)	JEDEC JESD22-A102, T_{amb}=121°C, p=15psig, 100% RH, t=96 hrs	_[2)]	-	-
A4	Temperature Cycling (TC)	JEDEC JESD22-A104, T_{amb}=-65°C to 150°C, 2000 cycles	3	77	0
A4a	Temperature Cycling Hot Test (TCHT)	JEDEC JESD22-A104, T=-65°C to 150°C, 1000 cycles, followed by wire pull on 5 parts	_[3)]	-	-
A4a alt	Temperature Cycling Delamination Test (TCDT)	JEDEC JESD22-A104, J-STD-035, T=-65°C to 150°C, 1000 cycles, followed by C-SAM inspection and wire pull	_[2) 3)]	-	-
A5	Intermittent Operational Life (IOL)	MIL-STD-750-1 Method 1037, T_{amb}=25°C, ΔTj≧100°C, ton=toff=2 min, t=2000 hrs	3	77	0
A5 alt	Power and Temperature Cycle (PTC)	JEDEC JESD22-A105, T=-40°C to x°C to obtain ΔTj≧100°C, ton=toff=2 min, t=1000 hrs	_[2) 4)]	-	-

Production Part Approval - Environmental Test Summary

(according to AEC-Q101-RevD & AEC-Q006-RevA)

Supplier	User Part Number				
Nexperia Germany GmbH	50V				
Name of Laboratory	**Part Description**				
Nexperia Q-Lab (HH)	NPN-Transistor in SOT8015				
Test #	**Test Description**	**Test Conditions**	**# Lots**	**# Tested**	**# Failed**
8	Unbiased Highly Accelerated Stress Test (UHAST)	JESD22 A-118, T=130°C, 85% RH, t=96 hrs	3	77	0
8 alt	Autoclave (AC)	JESD22 A-102, T=121°C, p=15psig, 100% RH, t=96 hrs	_[16)]	-	-
9	Highly Accelerated Stress Test (HAST)	JESD22 A-110, T=130°C, 85% RH, t=96 hrs, reverse biased at 80% of rated voltage	_[16)]	77	0
9 alt	High Humidity High Temperature Reverse Bias (H3TRB)	JESD22 A-101, T=85°C, 85% RH, reverse biased at 80% of rated breakdown voltage up to maximum 115V, t=2000 hrs	3	77	0
9a	High Temperature High Humidity Bias (HTHHB)	JESD22 A-101, T=85°C, 85% RH, parts forward biased	_[5)]	-	-
10	Intermittent Operational Life (IOL)	MIL-STD-750 Method 1037, T=25°C, ΔTj≧100°C, ton=toff=2 min, t=2000 hrs	3	77	0
10 alt	Power and Temperature Cycle (PTC)	JESD22 A-105,T=-65°C to x°C to obtain ΔTj≧100°C, ton=toff=2 min, t=1000 hrs	_[16) 17)]	-	-

Reliability Monitoring for types with CD not acc. to IEC 60664-1

All reliability tests are performed on FR4 PCBs

Reliability monitoring on quaterly base for several types from each group
Example quantities tested in 2015

					Group 1 NiFe, Cu plating matte Sn		Group 2 Cu alloy matte Sn		Group 3 Cu alloy, NiPdAu matte Sn	
AEC-Q101 Test	**Test on PCB**	**According to Standard**	**Conditions**	**Duration**	**Tested Products Quantity**	**Rejects**	**Tested Products Quantity**	**Rejects**	**Tested Products Quantity**	**Rejects**
Electrical Test Pre- and Post-Stress			Tamb = 25 °C	N/A	180,364	0	19,120	0	52,214	0
PC		JESD22-A113	Bake T_{amb} = 125 °C	24 hours	84,862	0	8,720	0	24,862	0
Preconditioning			Soak T_{amb} = 85 °C, RH = 85%	168 hours						
	yes		Reflow soldering	3 cycles						
TCT Temperature Cycling	yes	JESD22-A104	-55 °C to T_{jmax}	1000 cycles	21,351	0	2,400	0	6,631	0
AC Autoclave	yes	JESD22-A102	T_{amb} = 121 °C, RH = 100 % Pressure = 205 kPa (29.7 psia)	96 hours	21,440	0	1,680	0	6,400	0
H3TRB High Humidity High Temperature Reverse Bias	yes	JESD22-A101	T_{amb} = 85 °C, RH = 85%, V_R > 80 % of rated breakdown voltage	1000 hours	22,231	0	2,400	0	6,631	0
IOL Intermittent Operating Life	yes	MIL-STD-750 Method 1037	ton = toff, devices powered to insure ΔTj = 125 °C for 7500 cycles or	1000 hours	19,840	0	2,240	0	5,200	0

➔ ~30k units monitored in 2015 with 0 rejects

Creepage Distance in Standardisation Committees

Definition of Guideline for Automotive Applications

IEC60664-1 & IPC-2221 are based on material knowledge and technologies from the 1980´s or even earlier, Background is not well documented, partially contradicting statements

➔ Review and rework for automotive applications in a relatively well protecting housing is required.

Working groups DKE/AK 682.0.7 and DKE/AK 682.0.101 in frame of DKE/K 682 AVT für elektronische Baugruppen

DKE/AK 682.0.7 — Aufbau- und Verbindungstechnik in der Automobilelektronik

DKE/AK 682.0.101 — ad hoc Kriechstrecken und Kontaktabstände

members

Fraunhofer IPA	Stuttgart
TechnoLab	Berlin
KOSTAL Automobil	Dortmund
Robert Bosch	Schwieberdingen
Engineering Consultant	Seukendorf
HELLA	Lippstadt
ZESTRON Europe	Baar-Ebenhausen
Forvia	Lippstadt
Phoenix Contact	Blomberg
Nexperia	Hamburg
SEMIKRON	Nürnberg
Diehl Aerospace	Frankfurt am Main

Target of working group:
Guideline to apply IEC60664 / IPC-2221 for automotive applications

Summary

More electrical functions require higher PCB density and smaller products

- This is in conflict with
  - Distance requirements depending on application voltage (IEC60664-1)
  - Large package heatsink area required for cooling

The IEC 60664-1 needs to be adapted to today's application environments

- Billions of products delivered to market with smaller creepage distance than required underline the potential to interpret/adapt IEC60664-1

There is no easy answer for a safe design

- It will be application specific and needs cooperation between component and electronic device suppliers
- The VDE/ DKE standardization committees are a good platform to cooperate

Thank you!

Let‘s get in touch!

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